C. Software Compatibility with Future GSPs

Software written for the TMS34010 should run without modification on future versions of the GSP as long as a few simple guidelines are followed.

- The next version of the GSP will have a 32-bit data bus to external memory, which is twice the size of the TMS34010's data bus. To accommodate the change in bus width, certain internal register values will be expanded from 16 to 32 bits:
  - The COLOR0 and COLOR1 values in registers B8 and B9 will be valid throughout all 32 bits of each register, rather than just the 16 LSBs.
  - The PMASK register will be expanded from 16 to 32 bits, and will occupy memory addresses >C000 0160 to >C000 017F.
- Upward compatibility with these modifications will be ensured by treating the COLOR0, COLOR1, and PMASK values as 32 bits, although the TMS34010 will ignore the 16 MSBs of these values. Specifically, the value in the 16 LSBs of COLOR0 or COLOR1 that is required for the TMS34010 should be copied into the 16 MSBs as well.
- The 16-bit PMASK value that is required for the TMS34010 should be copied not only in addresses >C000 0160 to >C000 016F, but also in addresses >C000 0170 to >C000 017F. Note that writing to addresses >C000 0170 to >C000 017F in the TMS34010 will have no effect, and that reading these locations will return all 0s.
- Certain *reserved* bits in the TMS34010's I/O registers and status register may be assigned functions in future GSPs. To maintain upward compatibility, software written for the TMS34010 should maintain 0s in reserved register bits.
- If the CONVSP register is used for an instruction, the value in the SPTCH (B1) register should also be valid. That is, SPTCH and CONVSP should be set up to support the same source pitch value. Similarly, if the CONVDP register is used for an instruction, the value in the DPTCH (B3) register should also be valid. These steps will ensure software compatibility with future GSPs that may ignore the contents of CONVSP and CONVDP locations, and instead obtain all source and destination pitch information from the SPTCH and DPTCH registers alone.
- When the LINE instruction is used, register B13 should contain all 1s. This ensures that software using the LINE instruction is compatible with future versions of the GSP in which B13 will contain a line pattern consisting of 1s and 0s that are expanded to COLOR1 and COLOR0, respectively, as the line is drawn.
- All horizontal and vertical timing initialization should be performed by one routine; the HESYNC, HEBLNK, HSBLNK, HTOTAL, VESYNC, VEBLNK, VSBLNK, and VTOTAL may be assigned new addresses in future GSPs.